III-V MOSFETs for Future CMOS

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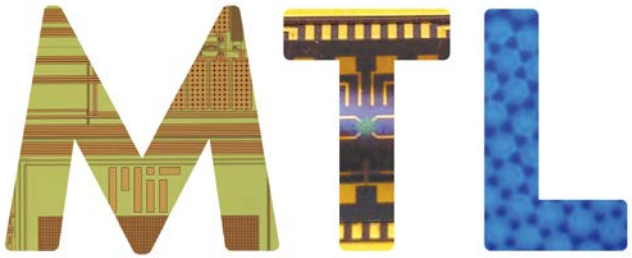

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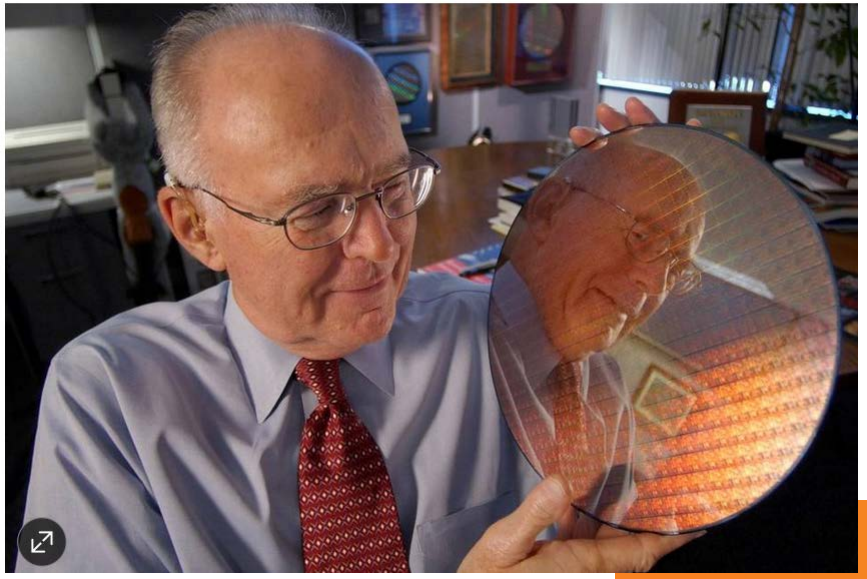
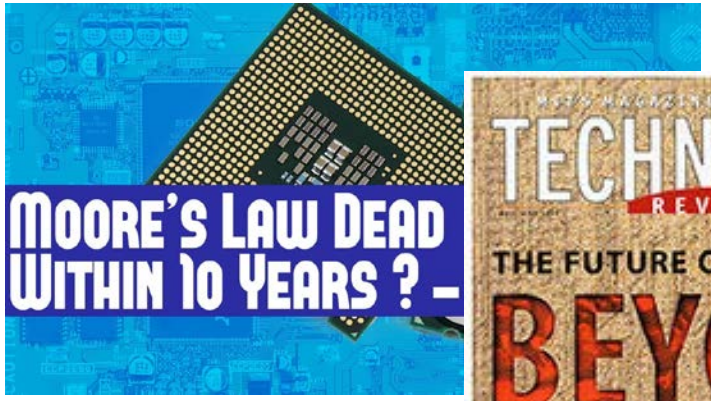
1. Moore's Law at 50: the end in sight?

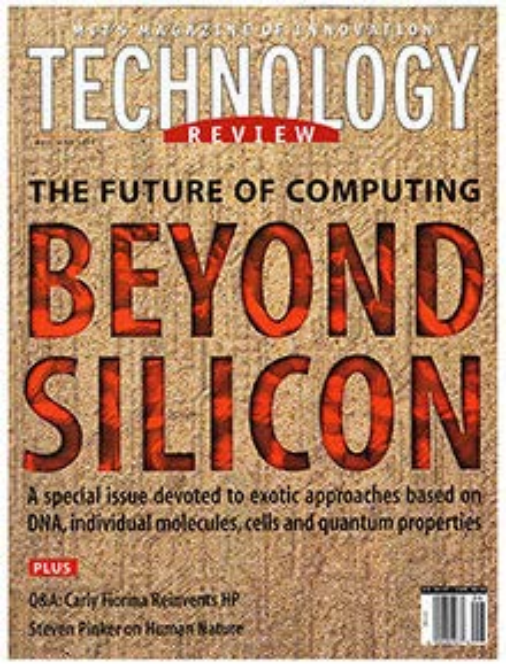
THE WALL STREET JOURNAL.

Moore's Law Is Showing Its Age

The prediction about squeezing transistors onto silicon has been revised again.

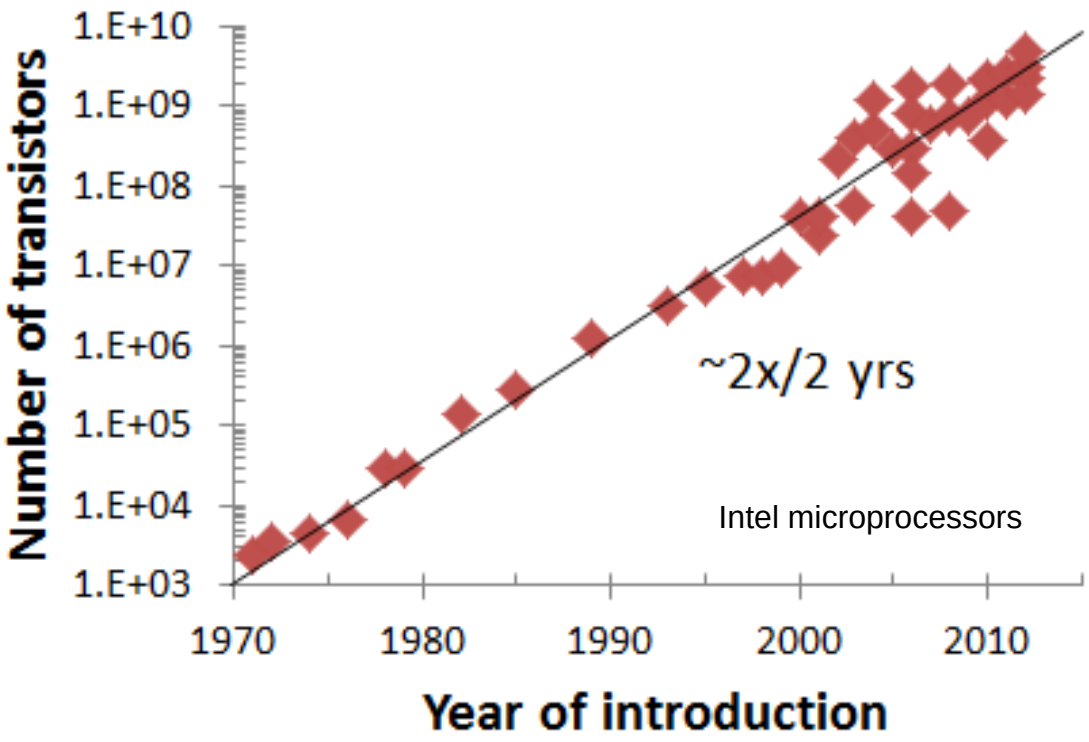


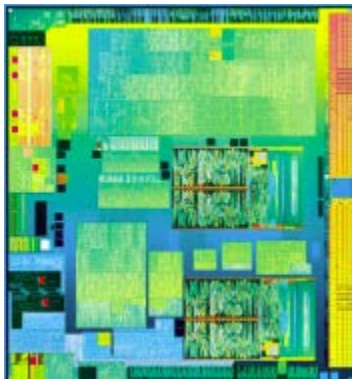




Moore's Law

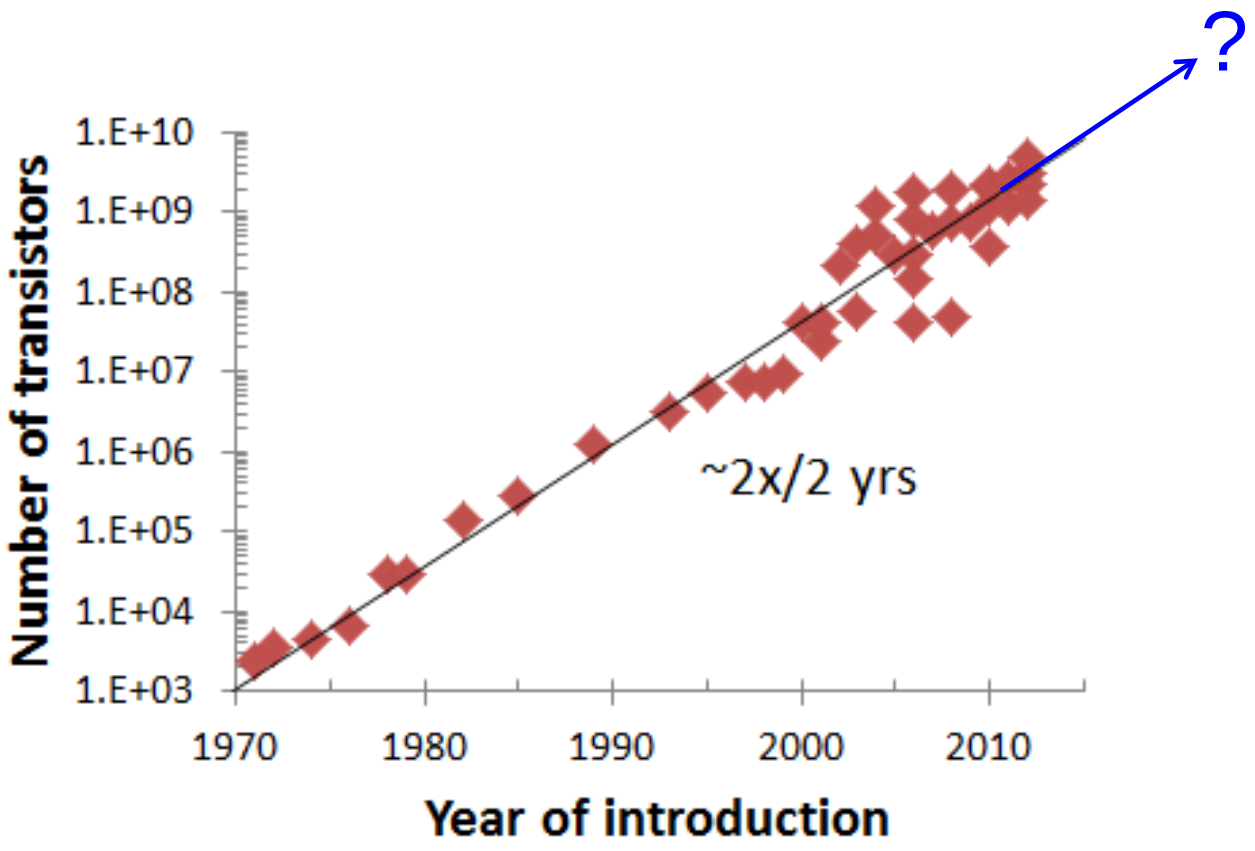
Moore's Law = exponential increase in transistor density





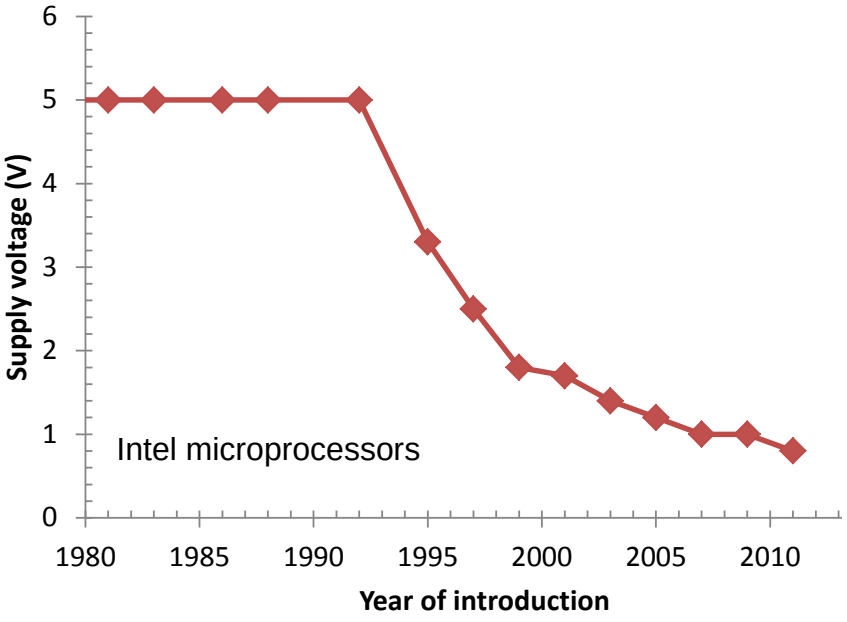
Moore's Law

How far can Si support Moore's Law?

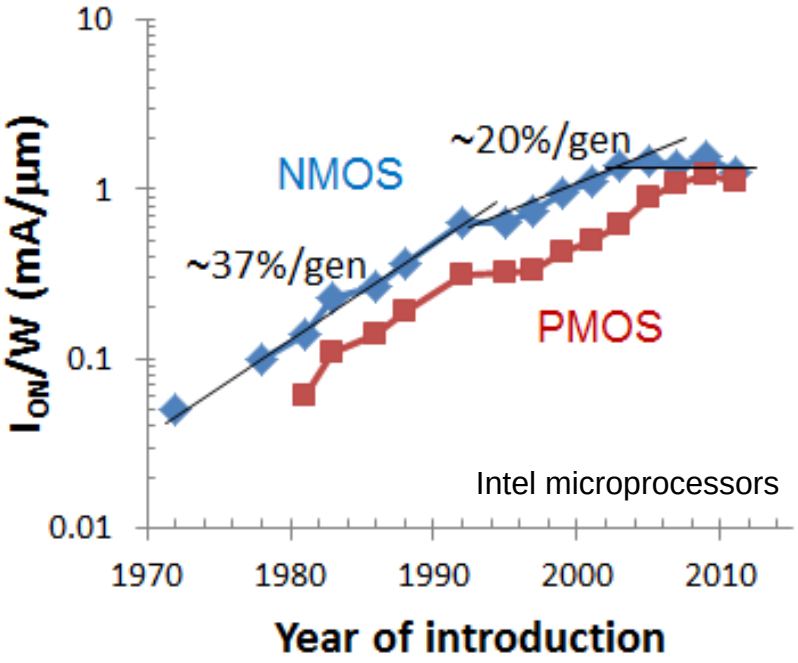


Transistor scaling → Voltage scaling → Performance suffers

Supply voltage:



Transistor current density (planar MOSFETs):

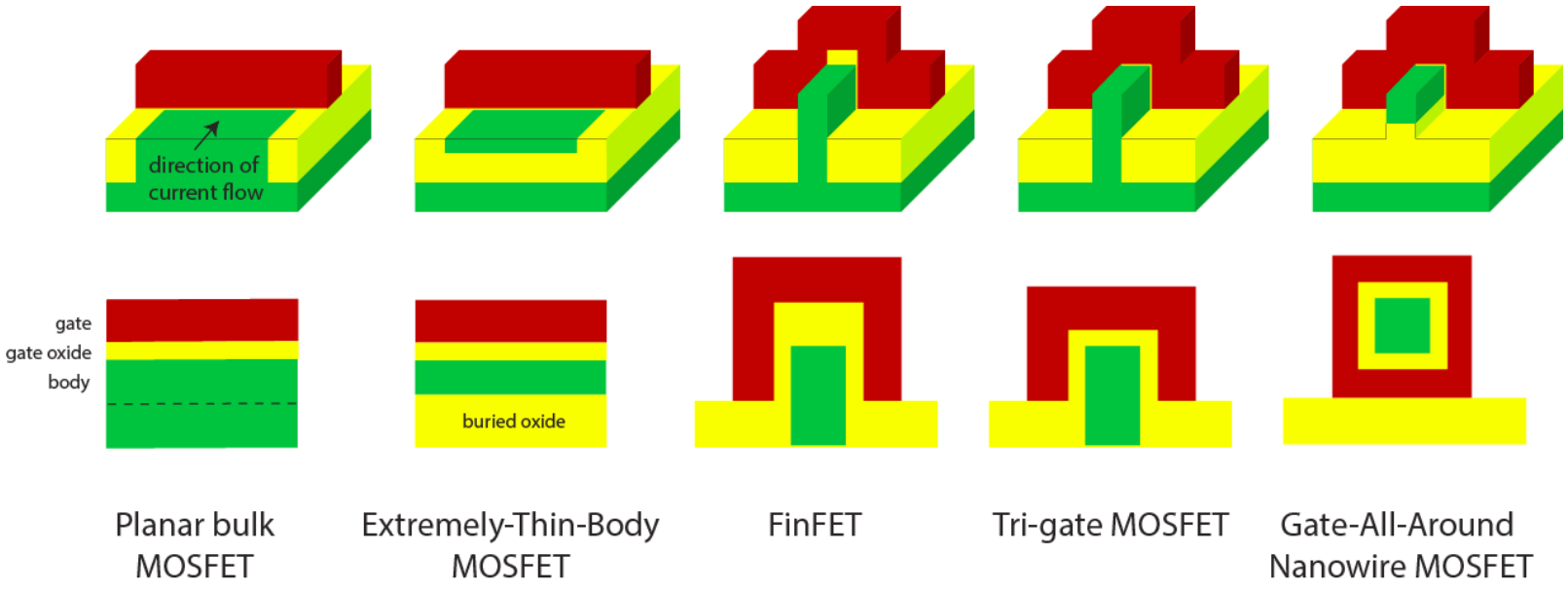


Transistor performance saturated in recent years


THE END IS NEAR.
YOU WISH.

Moore's Law: it's all about MOSFET scaling

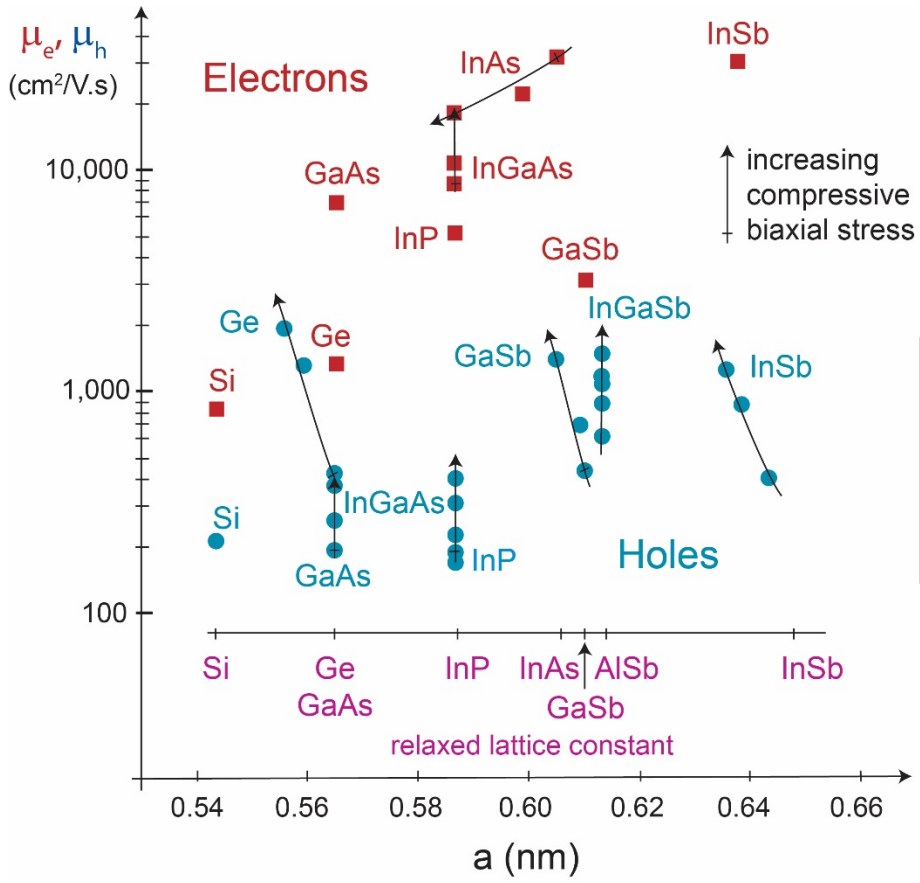
1. New device structures:



Enhanced gate control → improved scalability

Moore's Law: it's all about MOSFET scaling

2. New materials:



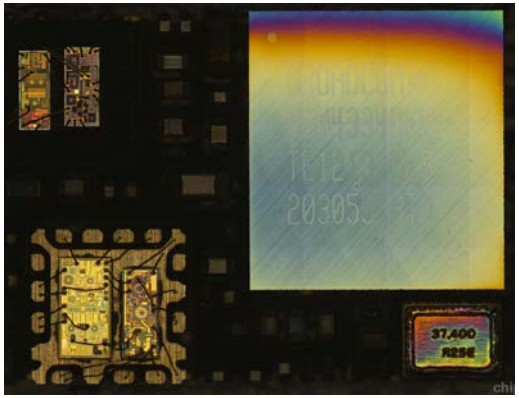
Si → Strained Si → SiGe → InGaAs

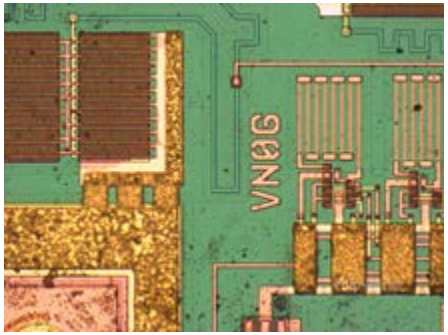
Si → Strained Si → SiGe → Ge → InGaSb

Future CMOS might involve two different channel materials with **two different relaxed lattice constants**!

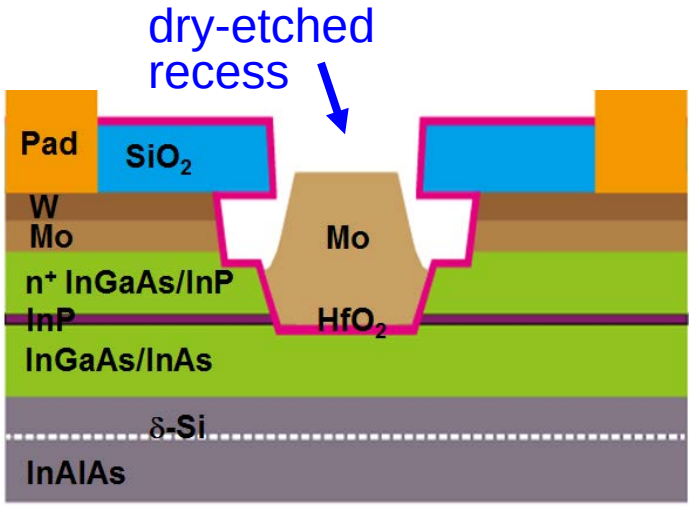
del Alamo, Nature 2011 (updated)

III-V electronics in your pocket!

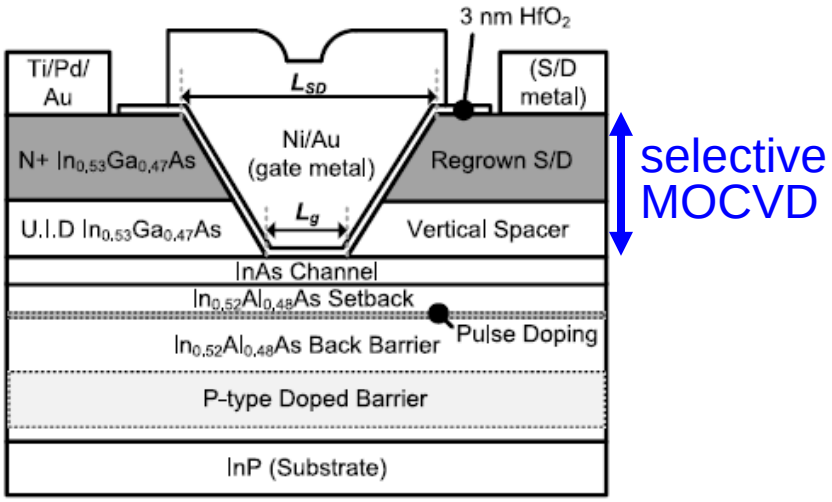




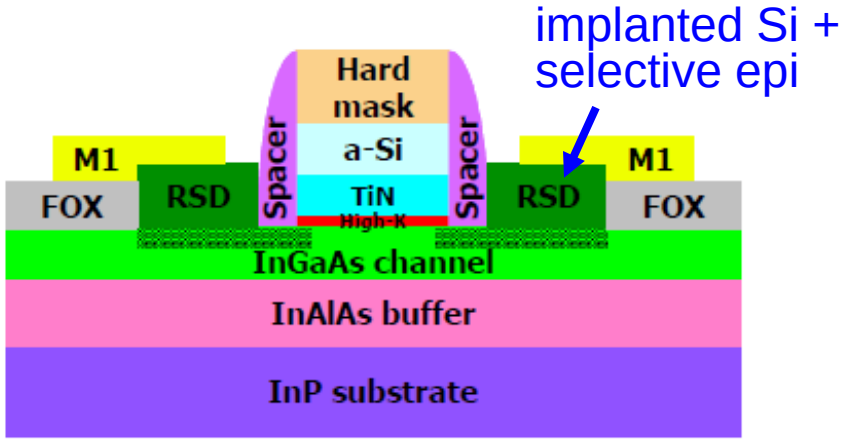
2. Self-aligned Planar InGaAs MOSFETs



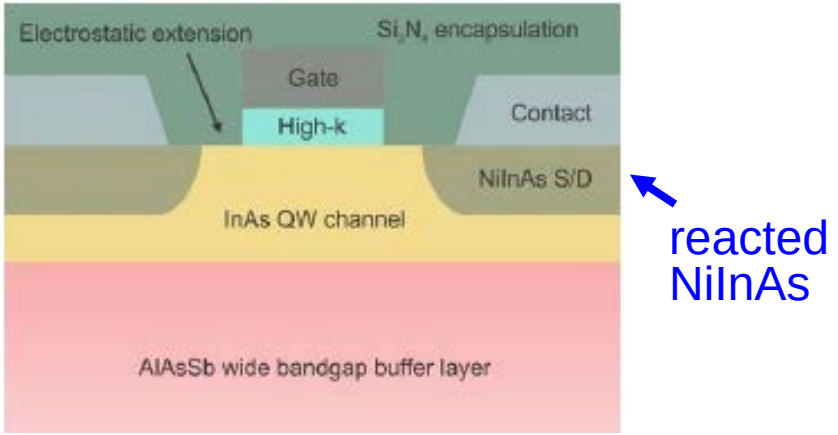
Lin, IEDM 2012, 2013, 2014



Lee, EDL 2014; Huang, IEDM 2014

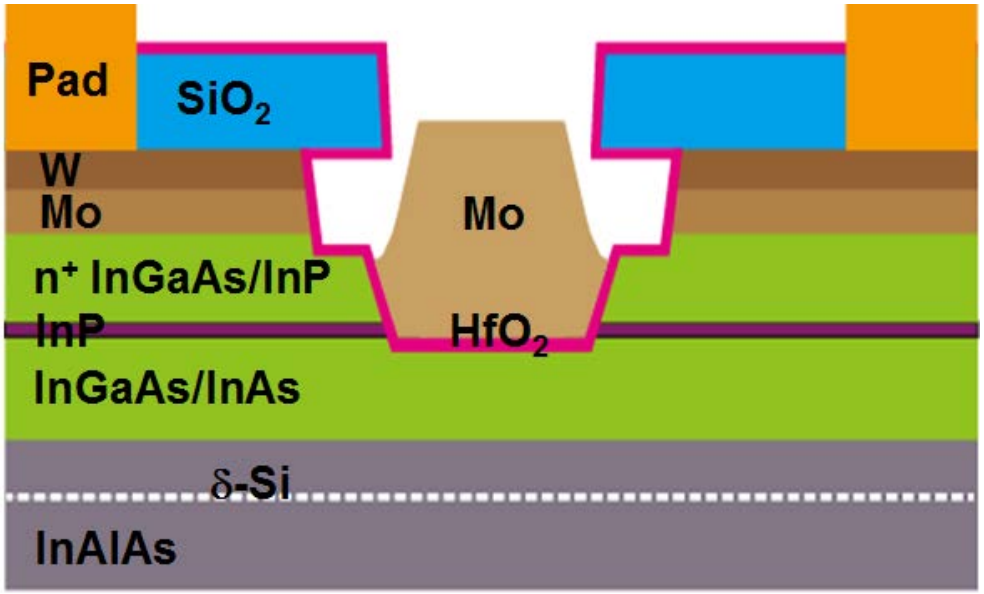


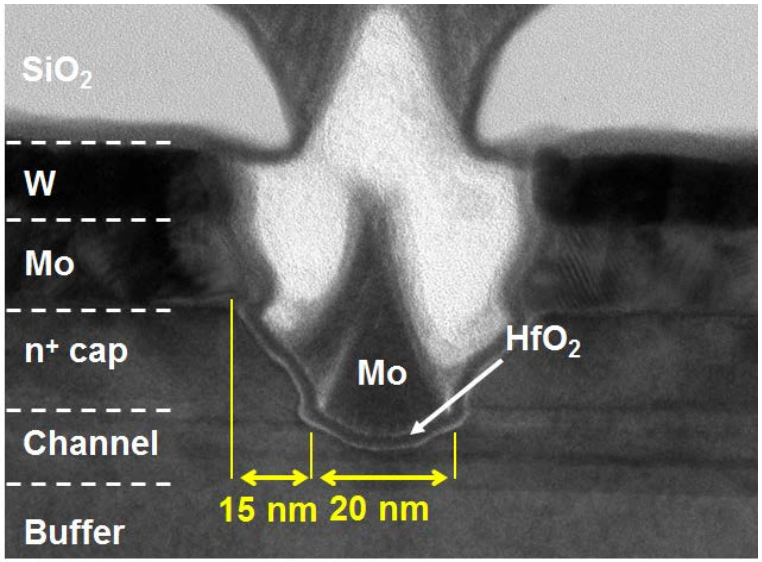
Sun, IEDM 2013, 2014



Chang, IEDM 2013

Self-aligned Planar InGaAs MOSFETs @ MIT

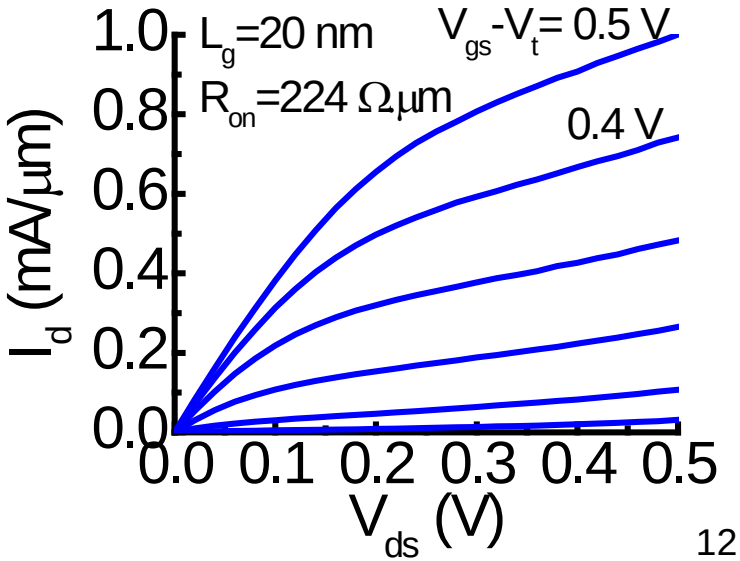




Lin, IEDM 2012, 2013, 2014

Recess-gate process:

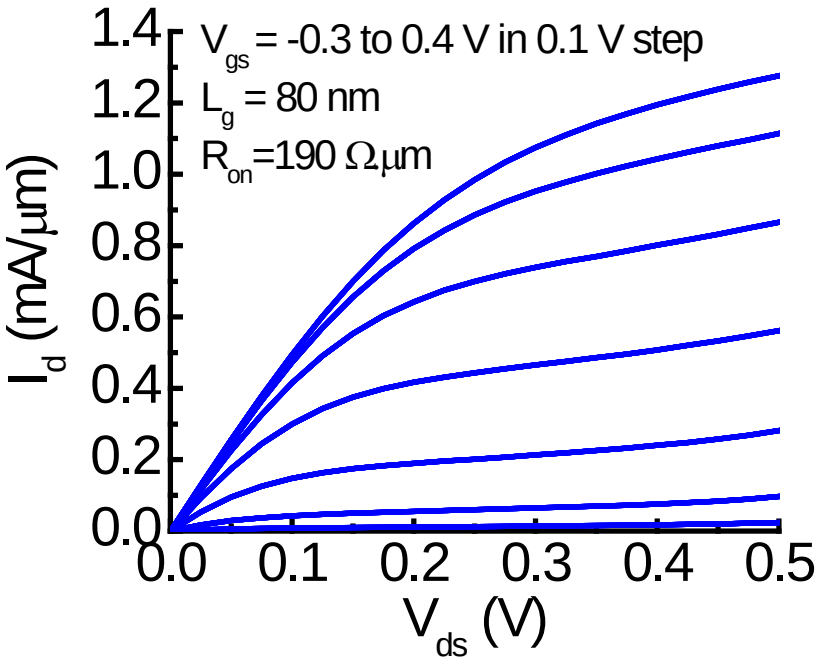
- CMOS-compatible
- Refractory ohmic contacts (W/Mo)
- Extensive use of RIE

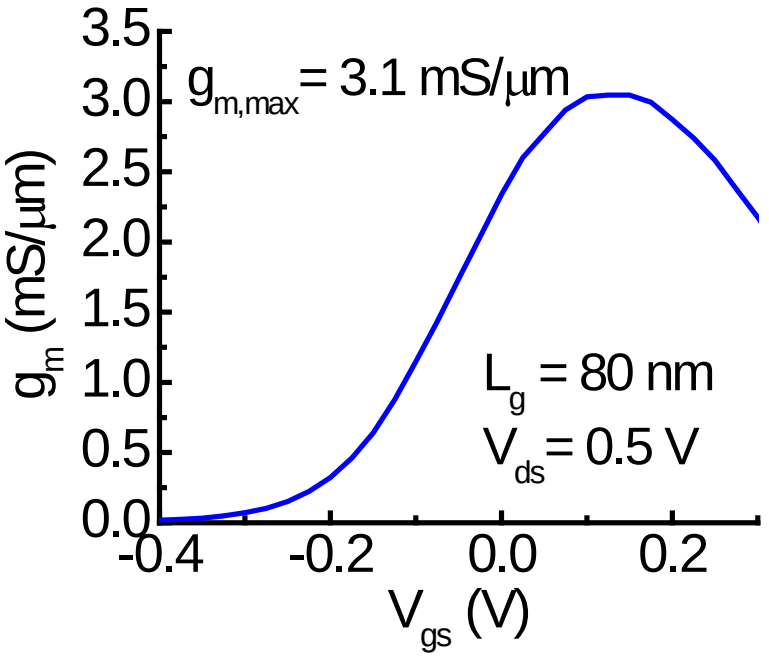


Highest performance InGaAs MOSFET

- Channel: $In_{0.7}Ga_{0.3}As/InAs/In_{0.7}Ga_{0.3}As$
- Gate oxide: HfO_2 (2.5 nm, EOT~ 0.5 nm)

L_g =80 nm, t_c=9 nm



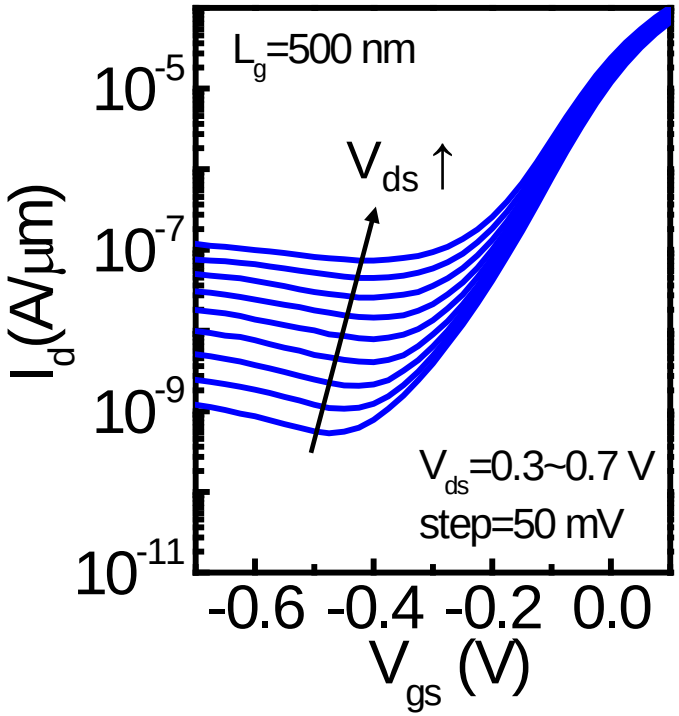


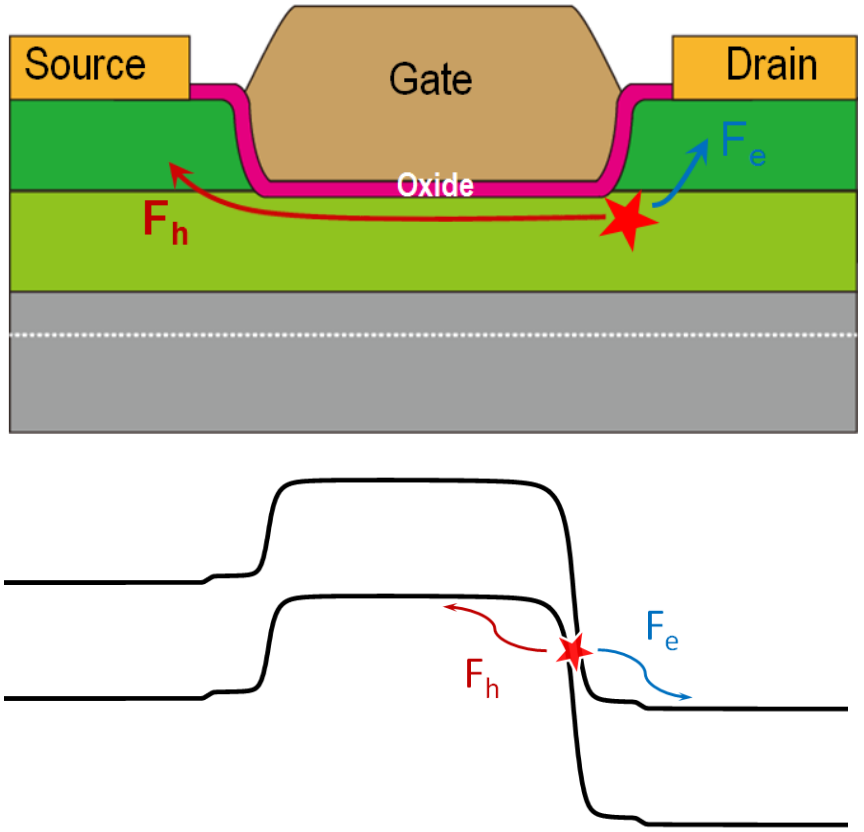
- Record $g_{m,max}$ = 3.1 mS/μm at V_{ds}= 0.5 V
- R_{on} = 190 Ω.μm

Lin, IEDM 2014

Excess OFF-state current

Transistor fails to turn off:



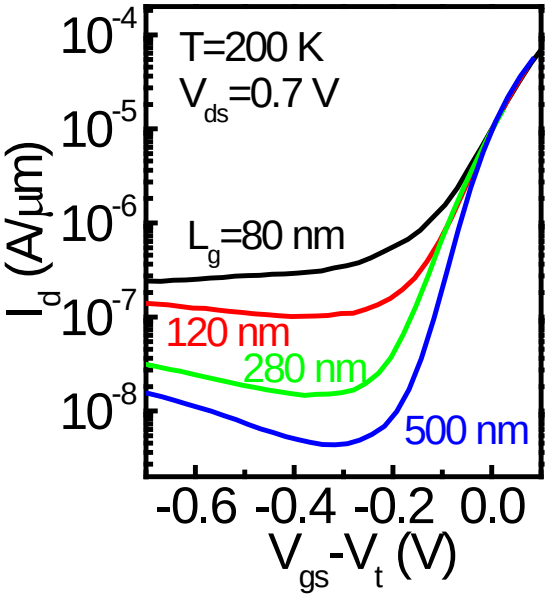


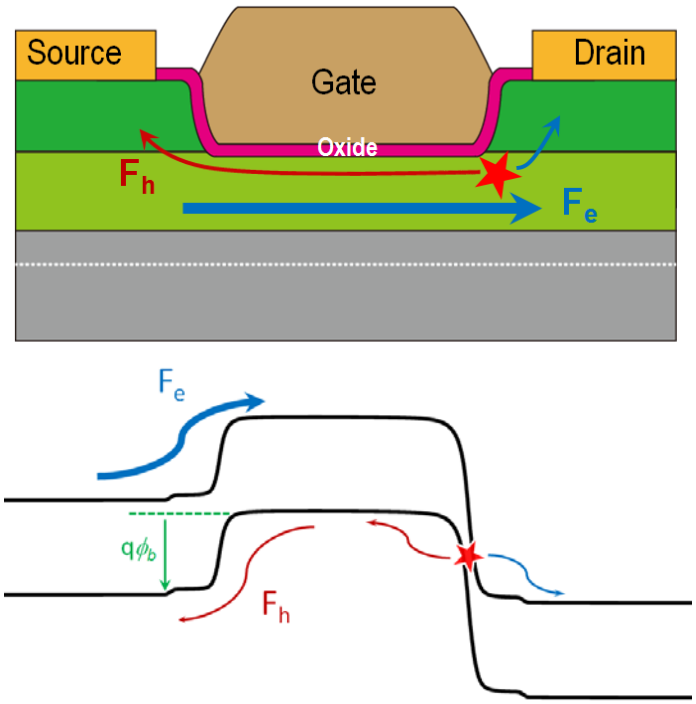
OFF-state current enhanced with V_{ds}

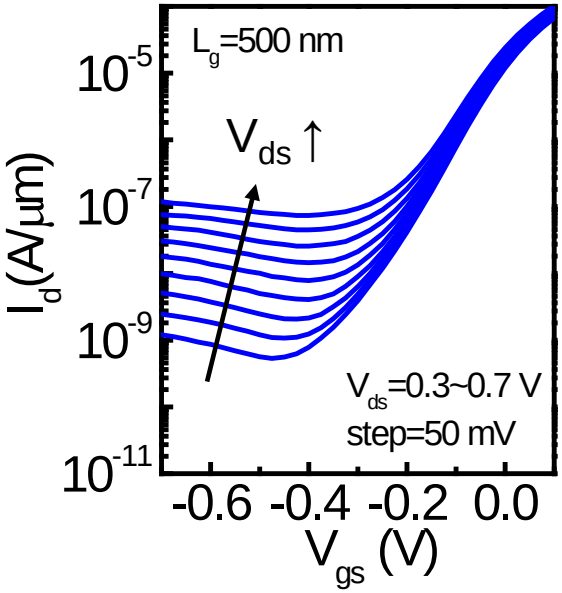
→ *Band-to-Band Tunneling (BTBT) or Gate-Induced Drain Leakage (GIDL)*

Lin, IEDM 2013

Excess OFF-state current



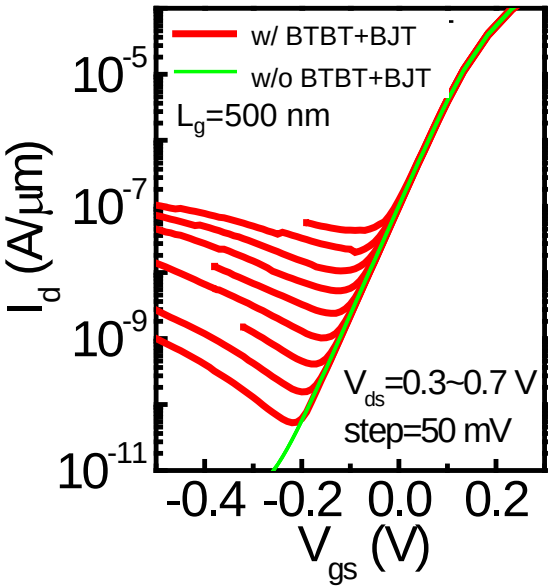




Lin, EDL 2014

Lin, TED 2015

Simulations

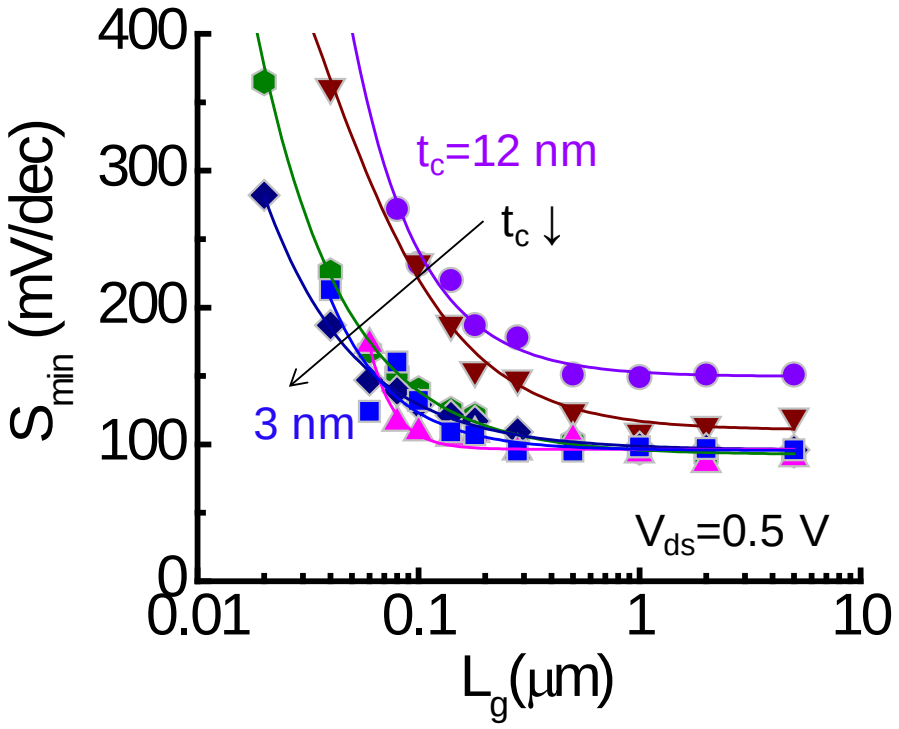


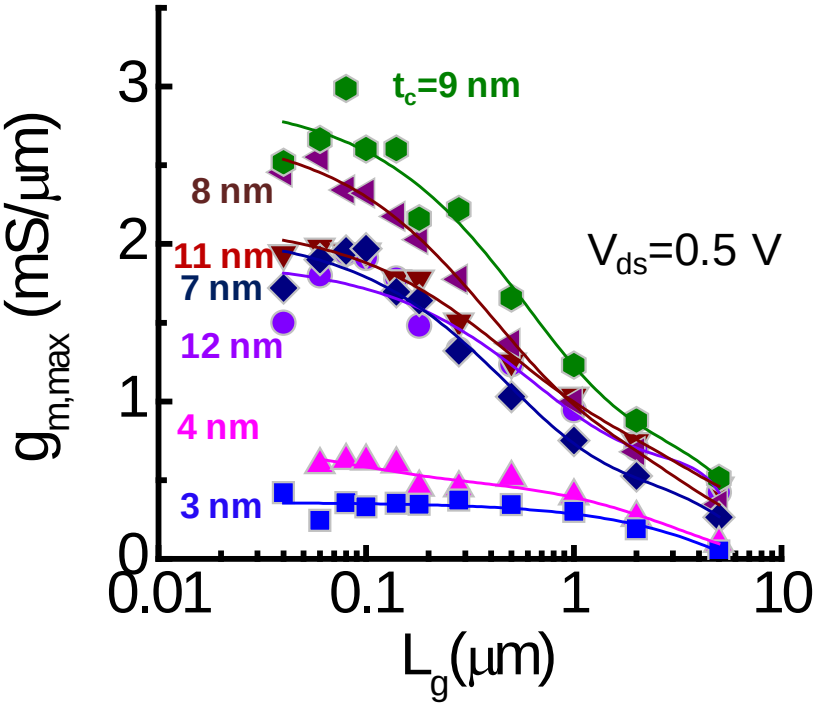
L_g↓ → OFF-state current ↑

→ additional *bipolar gain effect due to floating body*

Planar InGaAs MOSFET scaling

Lin, IEDM 2014
Lin, TED 2015



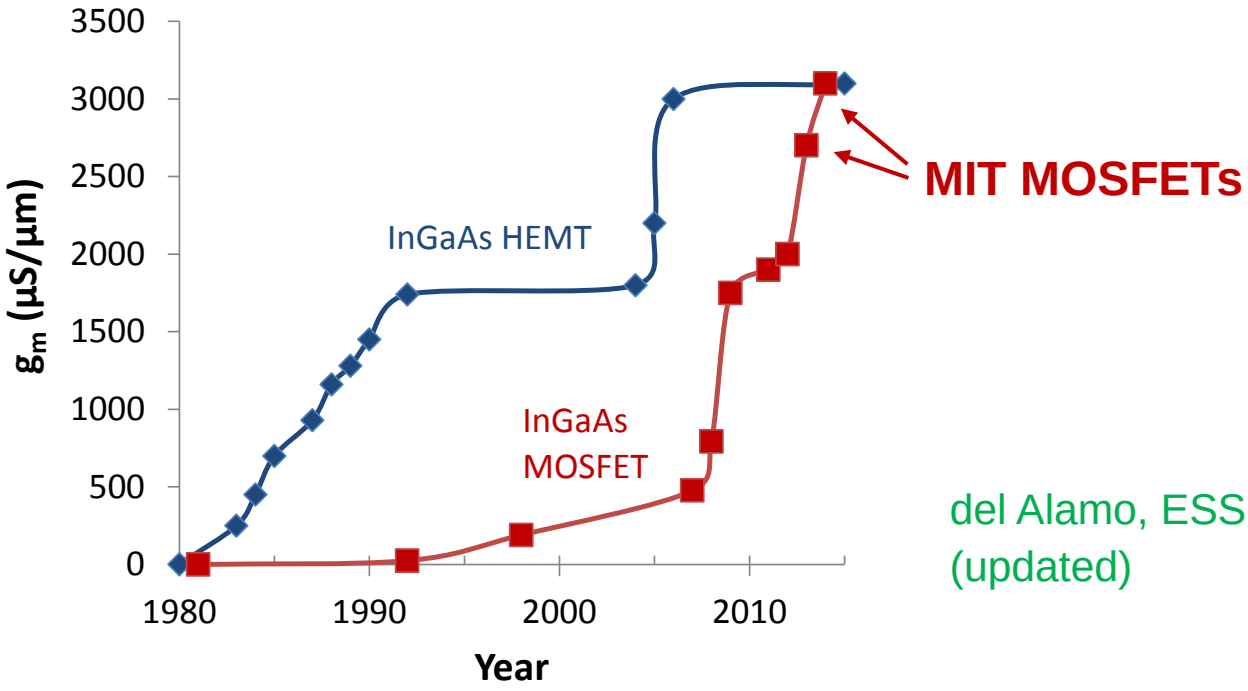


- t_c ↓ → S ↓ but also $g_{m,max}$ ↓
- Even at t_c=3 nm, $L_{g,min}$~40 nm

→ planar MOSFET at limit of scaling

Benchmarking: g_m in MOSFETs vs. HEMTs

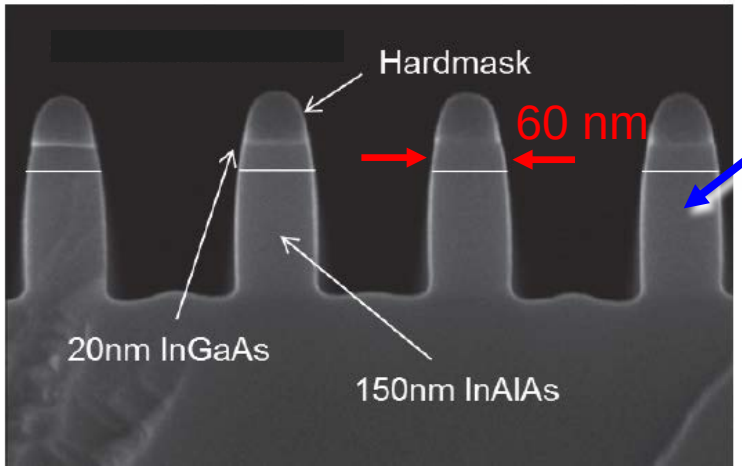
g_m of InGaAs MOSFETs vs. HEMTs (any V_{DD}, any L_g):



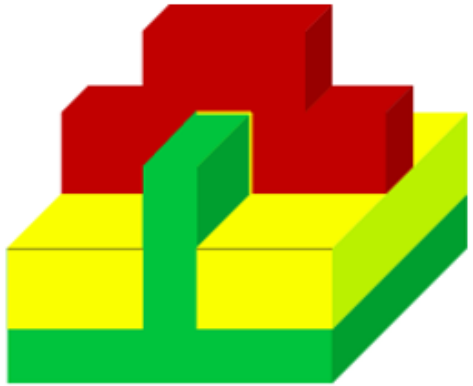
del Alamo, ESSDERC 2013 (updated)

- Very rapid recent progress in MOSFET g_m
- Best MOSFETs now match best HEMTs
- No sign of stalling → more progress ahead!

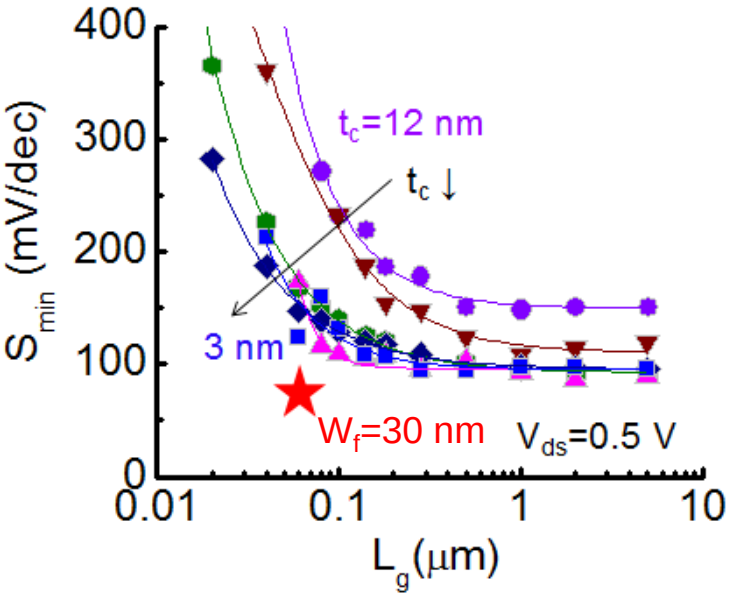
3. InGaAs FinFETs and Trigate MOSFETs

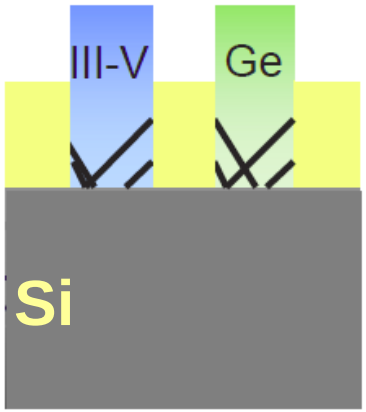


Dry-etched fins

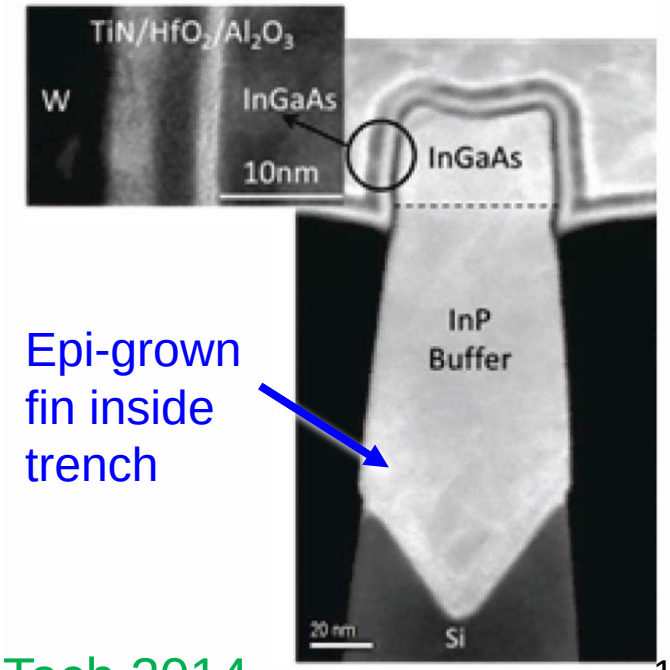


Kim, IEDM 2013





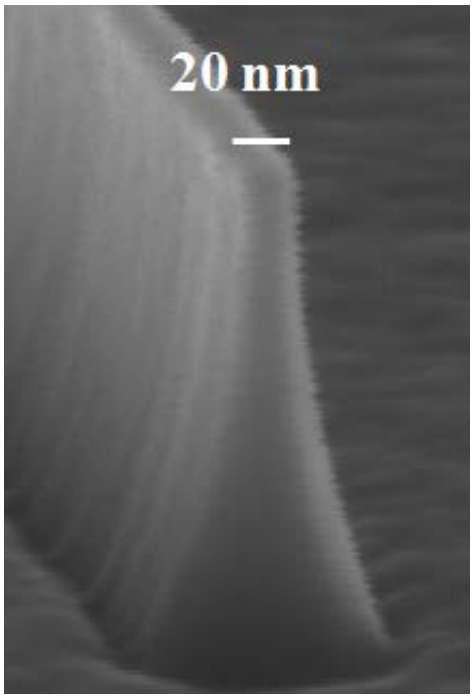
Aspect-Ratio Trapping

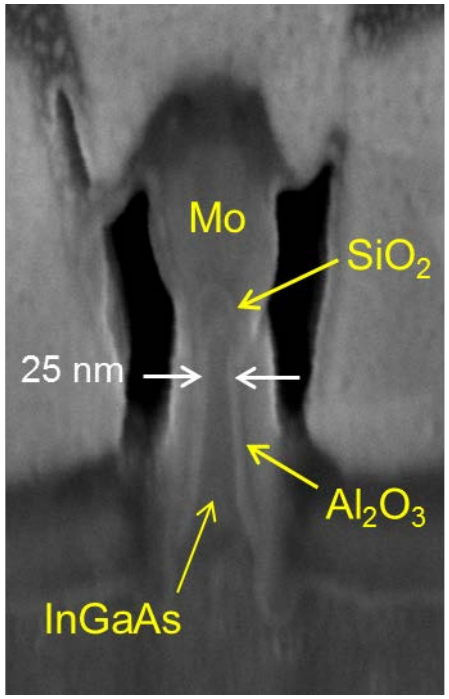


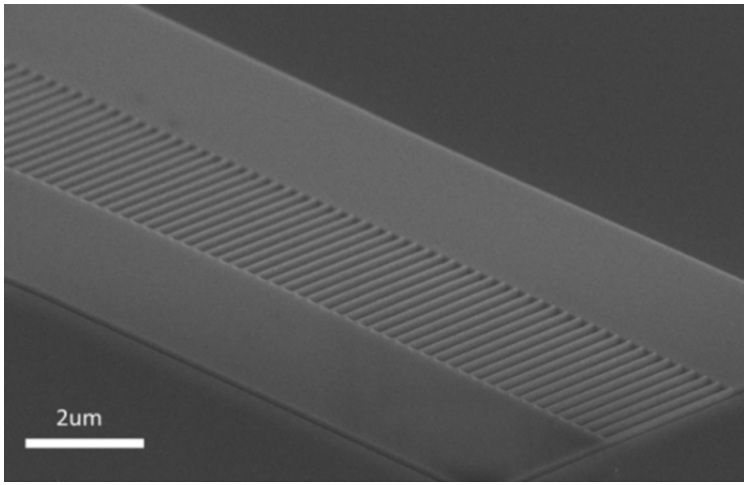
Epi-grown fin inside trench

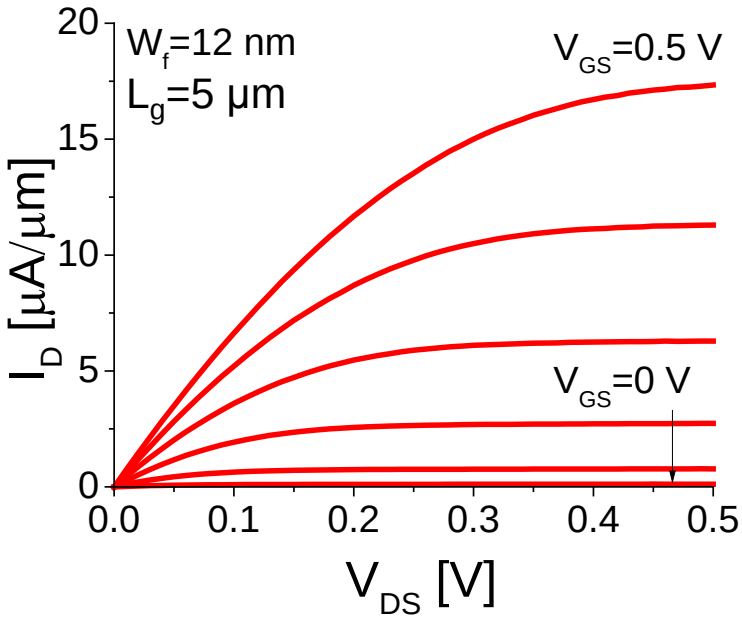
Waldron, VLSI Tech 2014

InGaAs FinFETs @ MIT





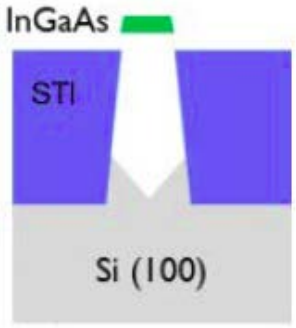


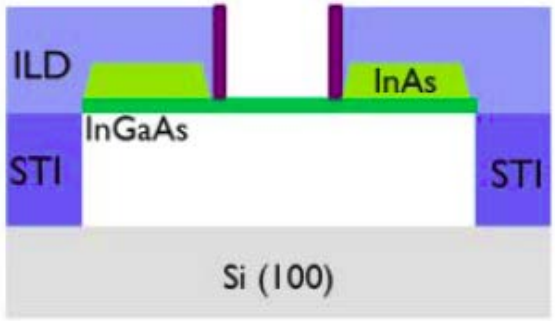


Fin etch by RIE

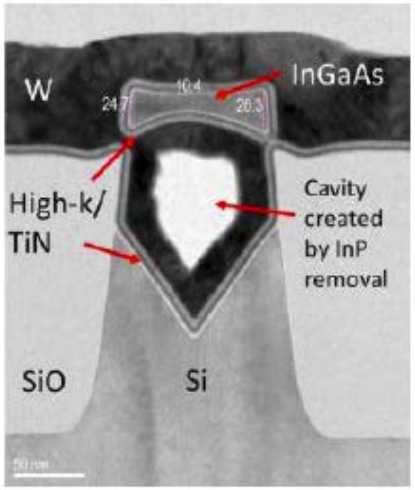
Vardi, DRC 2014, EDL 2015, IEDM 2015

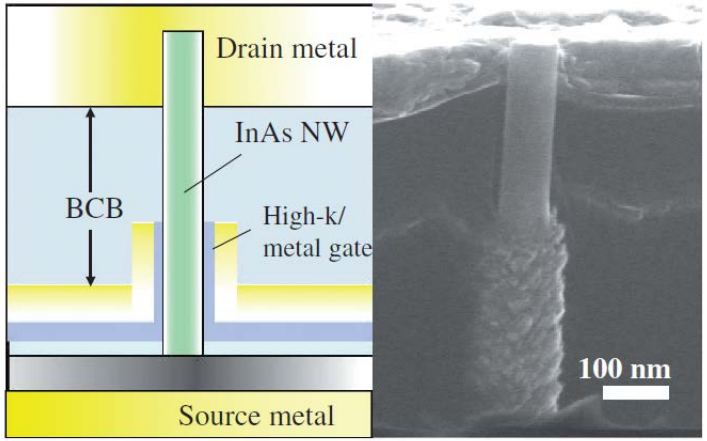
4. Nanowire InGaAs MOSFETs



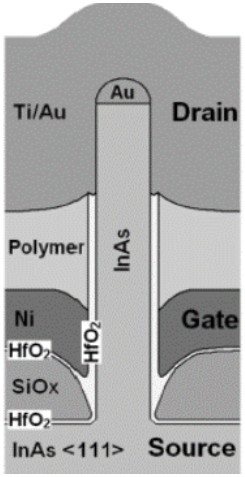


Waldron, EDL 2014

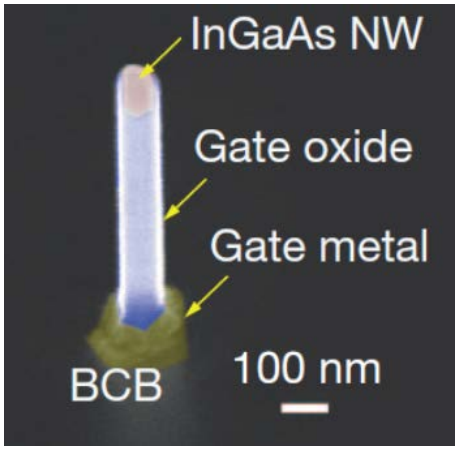




Tanaka, APEX 2010



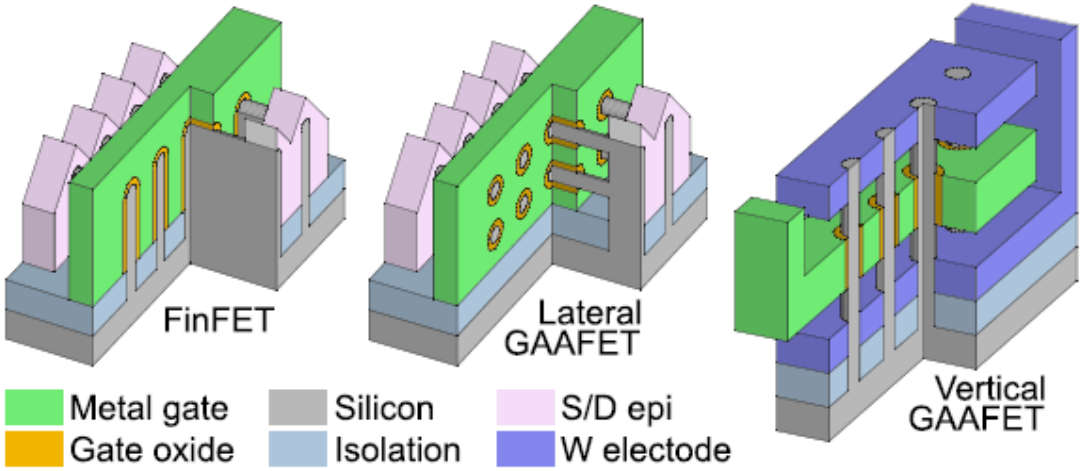
Persson, EDL 2012

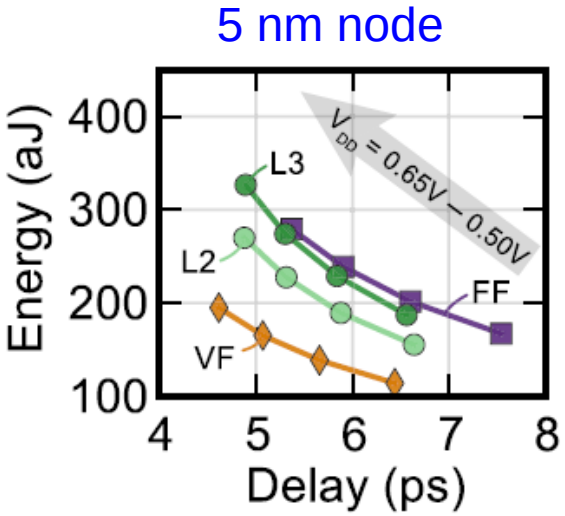


Tomioka, Nature 2012

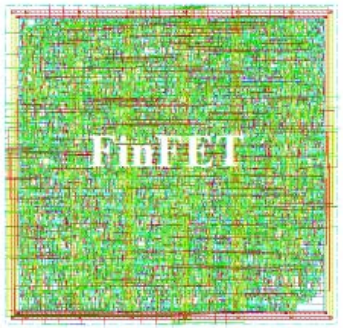
Nanowire MOSFET: ultimate scalable transistor

Lateral vs. Vertical Nanowire MOSFETs





Yakimets, TED 2015
Bao, ESSDERC 2014

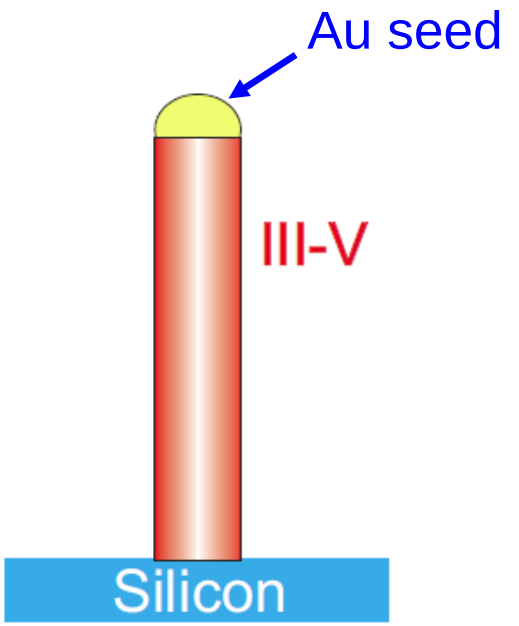


30% area reduction in 6T-SRAM
19% area reduction in 32 bit multiplier

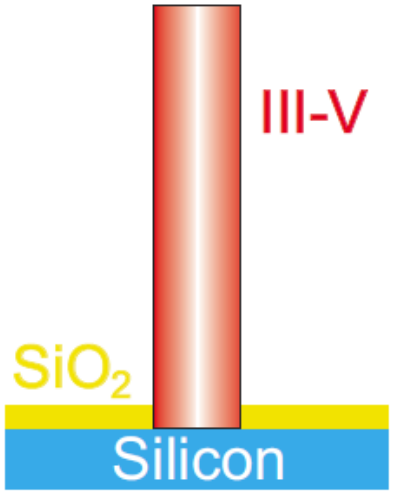
Vertical NW: uncouples footprint scaling from L_g and L_c scaling

→ power, performance and area gains wrt. Lateral NW

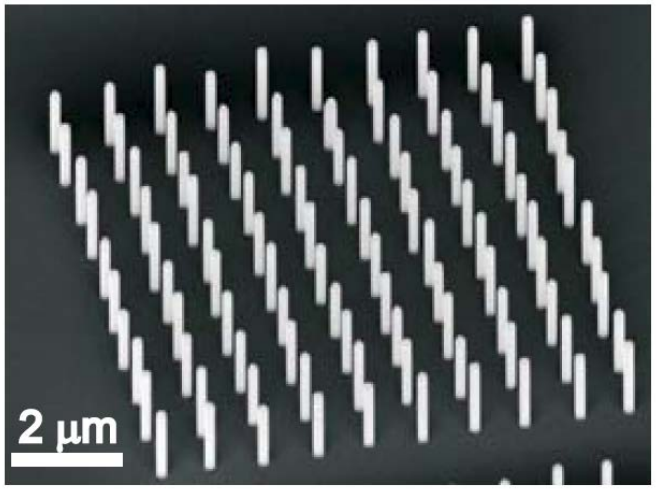
InGaAs Vertical Nanowires on Si by direct growth



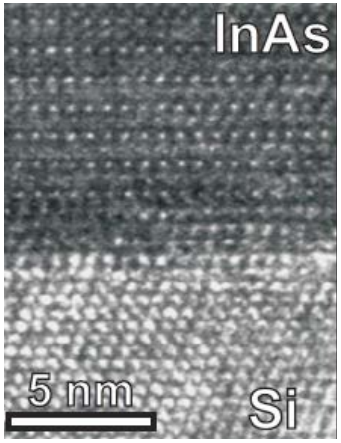
Vapor-Solid-Liquid (VLS) Technique



Selective-Area Epitaxy



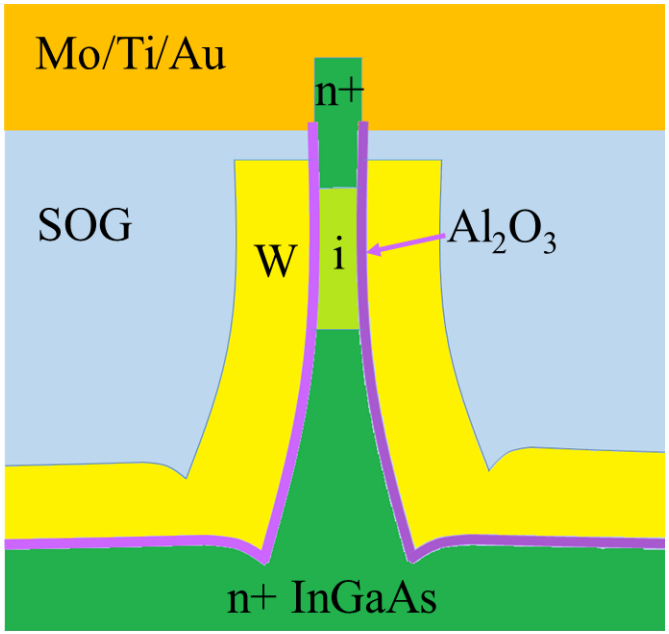
InAs NWs on Si by SAE



Björk, JCG 2012

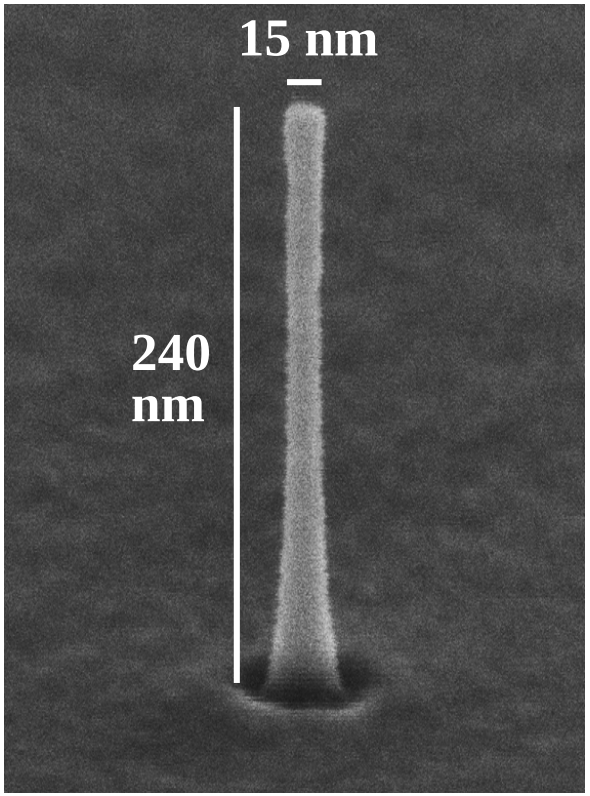
Riel, MRS Bull 2014

InGaAs VNW-MOSFETs fabricated via top-down approach @ MIT



Key enabling technologies:

- $BCl_3/SiCl_4$/Ar RIE
- digital etch

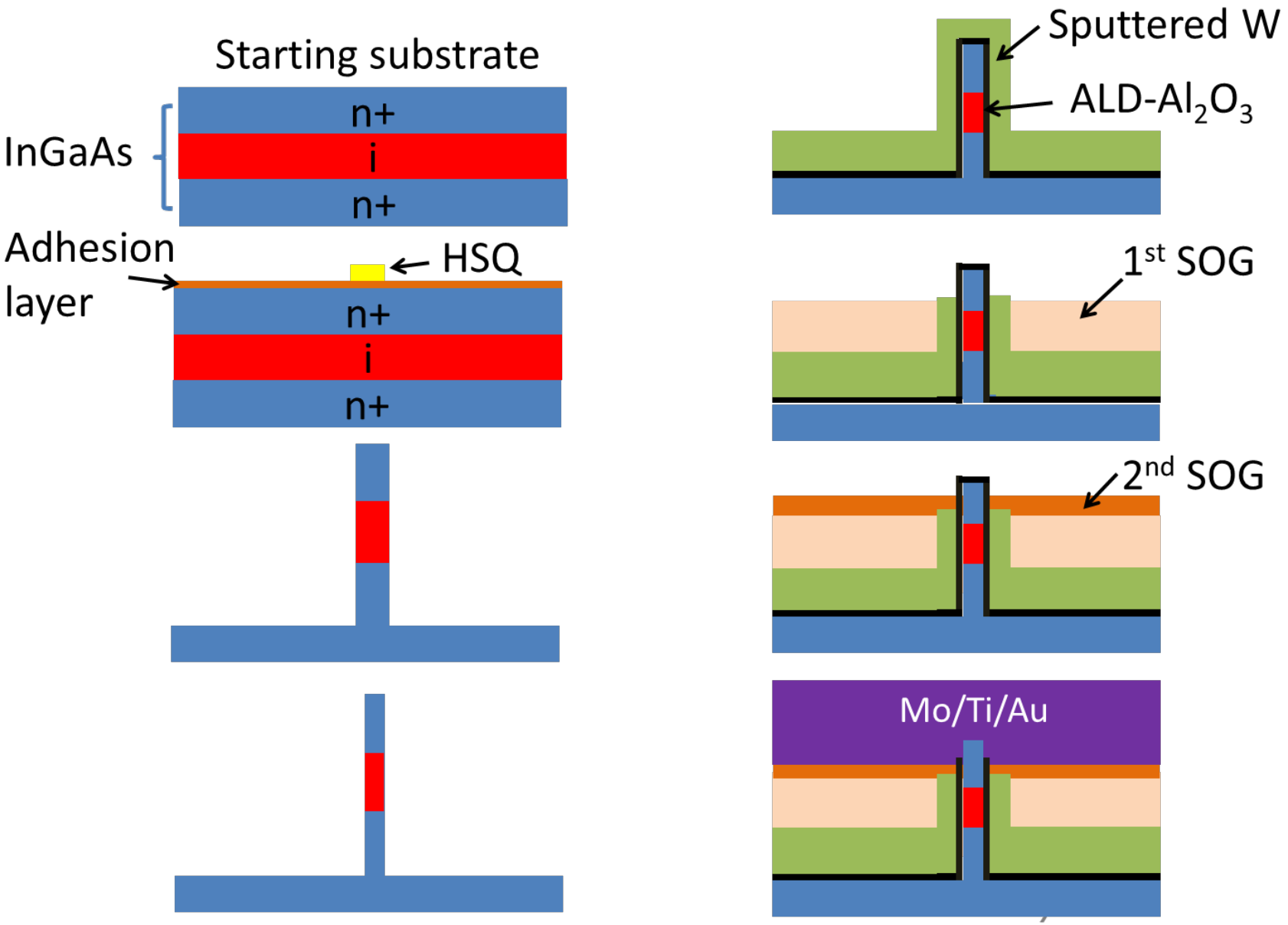


Zhao, IEDM 2013

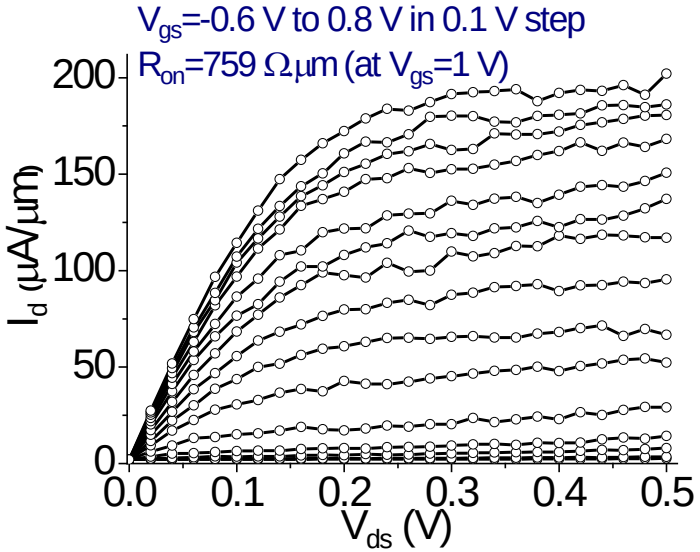
Top-down approach: flexible and manufacturable

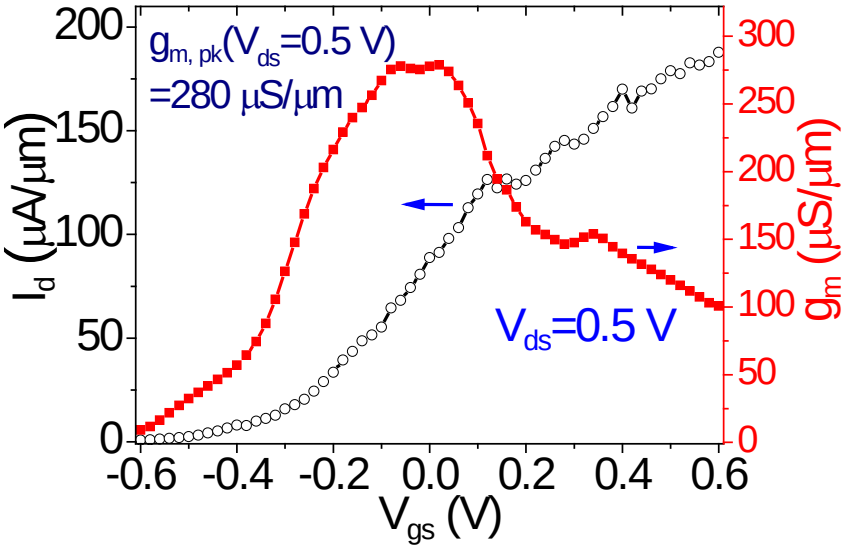
Tomioka, Nature 2012
Persson, DRC 2012

Process flow



D=30 nm NW-MOSFET



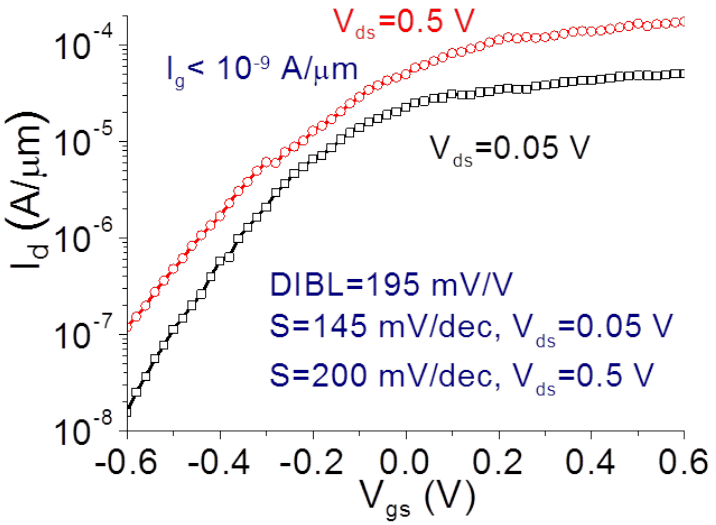


Single nanowire MOSFET:

- D=30 nm
- L_{ch}= 80 nm
- 4.5 nm Al_2O_3 (EOT = 2.2 nm)

At V_{DS}=0.5 V:

- $g_{m,pk}$=280 μS/μm
- R_{on}=759 Ω.μm



Zhao, IEDM 2013

Conclusions

1. Great recent progress on planar, fin and nanowire III-V MOSFETs
2. Vertical Nanowire III-V MOSFET: superior scalability and power/performance characteristics
3. Vertical Nanowire n- and p-type III-V MOSFET: plausible path for co-integration on Si
4. Many demonstrations of InGaAs VNW MOSFETs by bottom-up and top-down approaches
5. Many issues to work out…

A lot of work ahead but… exciting future for III-V electronics